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Development of Sensitive Lock in Amplifier for Electron Spin Resonance Spectrometer

K.SHANTI

Dept. of Physical Science, Kakatiya Institute of Technology & Science, Warangal (A. P)

ABSTRACT

A Linear Monolithic four quadrant Analog Multiplier has been used for the detection of electron spin resonance signals; in connection with a phase lock loop. The detection system employs an audio frequency modulation of the magnetic field followed by a phase sensitive detector where in analog Multiplier is used.

KEYWORDS:

Lock In amplifier, Phase, Sensitive Detection, Wide bond filter, Analog Multipliers, Phase Locked loop, ESR Signal Channel, Auxiliary amplifier & Low Pass Filter, Input Impedance & Output Impedance , Output Time Constant, Frequency of Operation, Linearity.

In Practical Measurements the signal information is always accompanied by an unwanted proportion of noise which is normally random and uncorrelated. The noise which is generated either from the source or in the signal recovery system limits the ultimate sensitivity of measurement.

A lock in Amplifier has a fundamental capability of recovering signal several orders of Magnitude below the input noise level. It extracts the signal from the noise by multiplying the signal input voltage with a reference voltage and filtering the output with a low pass filter of time constant. The noise equivalent bandwidth of this filter is $\Delta f_{out} = \Delta T$. Thus if the time constant is varied from 10 ms to 100 s Δf_{out} can be varied from 25 Hz to 0.0025 Hz and because of the narrow band width, there is a reduction in the noise power.

The AC to DC conversion in a Lock in amplifier is achieved through a phase sensitive detection (PSD), allowing narrow band width detection normally up to .001 Hz with stabilization

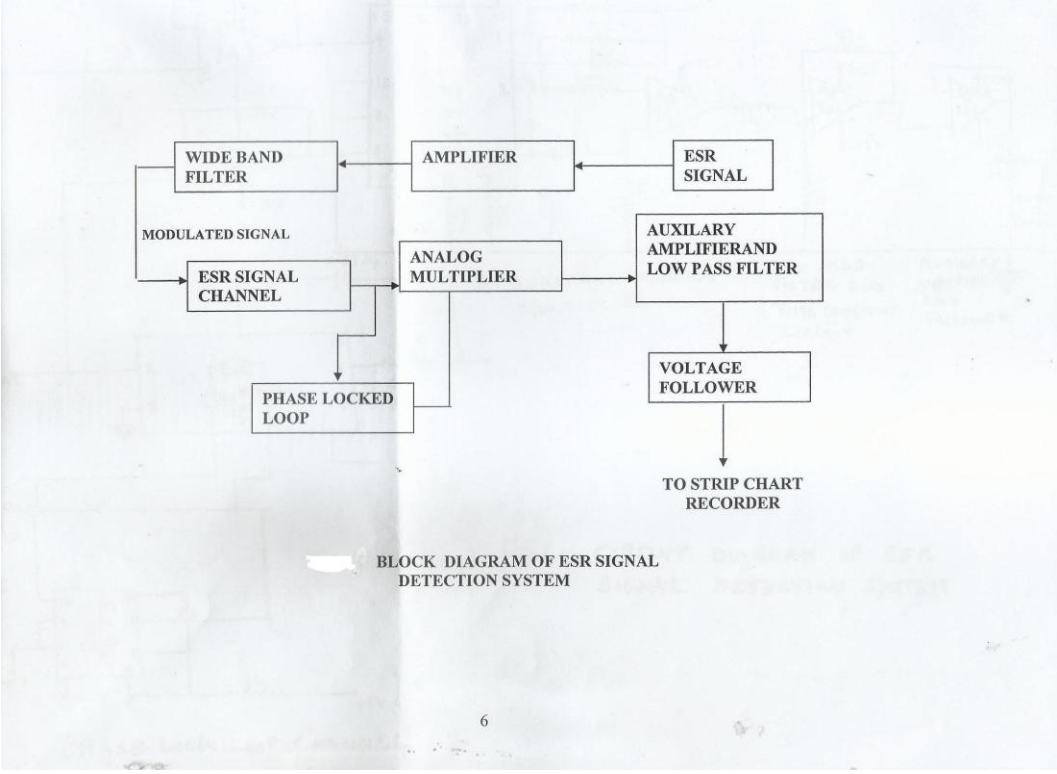
measured in parts per million. This method requires signal to be modulated at a discrete frequency after initial amplification and wide band filtering, the modulated signal is synchronously detected using reference signal to form the product in a multiplier circuit. While the noise spectrum is spread over a wide range of frequencies. The PSD responds only to the Input frequency centered at the reference frequency which is the desired signal and provides the needed noise rejection.

An Analog Multiplier is used as a phase sensitive detector since it can multiply the ESR signal voltage with the reference voltage. The product can be conveniently expressed in terms of a harmonic series from which the DC contribution can be extracted, the higher order frequencies being removed by a low pass filter.

$$V_{out} = K E_s E_r \cos\theta$$

Where E_s, E_r denote the signal and reference voltage of same frequency while θ is the phase angle between them. Here K is an appropriate scale factor chosen for the multiplier. The above equation gives the basic equation for the PSD system based upon analog signals and it expresses linearity and sensitivity. In an ESR experiment the amplitude E_r of the reference signal is always kept constant. The Phase difference θ between the signal and reference channel is normally made zero by a phase shifter in the reference channel. The signal amplitude is maximized by making $\cos\theta$ unity and the detector then produces a bipolar linear output related to E_r of the modulated ESR signal.

In the phase sensitive detection system, the reference is derived from the signal through a phase lock loop[PLL] . The following figure shows the block diagram of an Electron Spin Resonance [ESR] signal detection system.



BLOCK DIAGRAM OF ESR SIGNAL DETECTION SYSTEM

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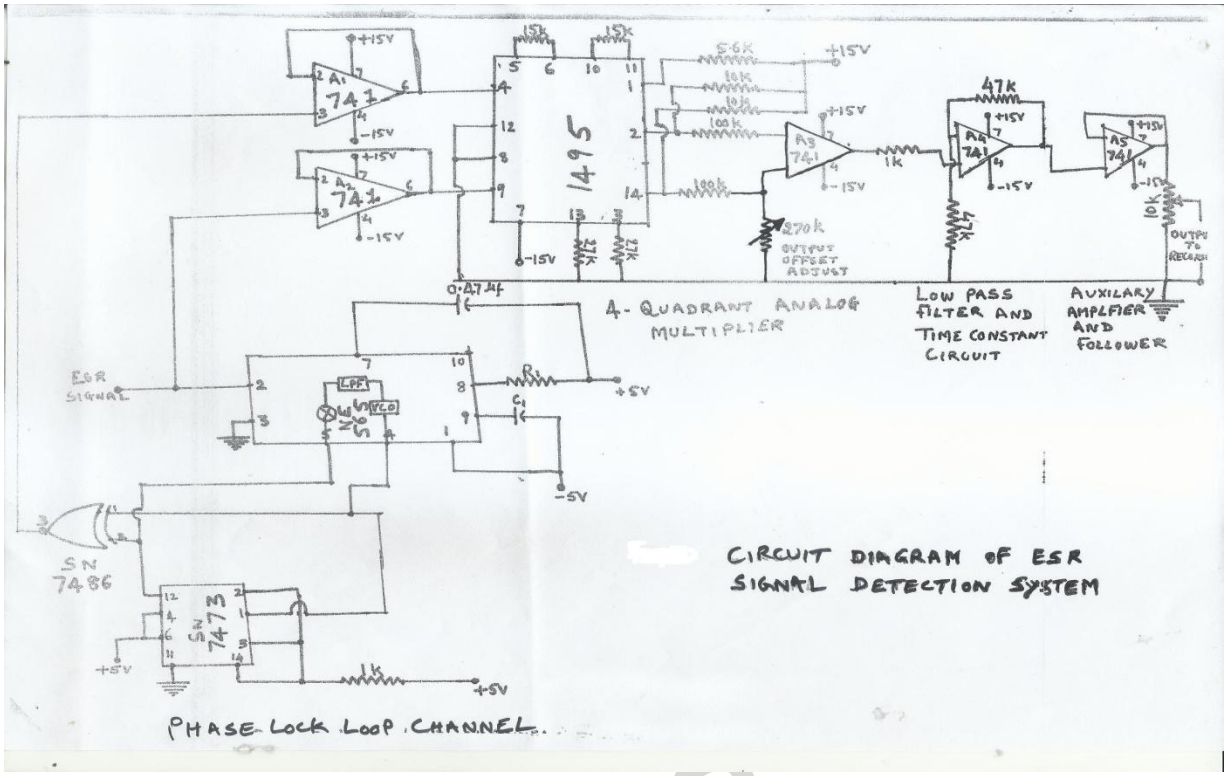
The signal consists of a low noise preamplifier with a maximum gain of 1000 followed by a narrow band amplifier. The narrow band amplifier uses the operational amplifier µA 741 and employs a twin – T-filter in its feedback loop. The output of this stage is also fed to the multiplier. The multiplier output is fed to the low pass filter of variable time constant, before going to the strip chart recorder.

The operational Amplifiers A1 and A2 in are connected as voltage followers.



The high input impedance of the follower avoids loading of the signal and reference source and related voltage dividers, also their very low output impedance is necessary to preserve the gain accuracy of the following stage. A3 converts the differential voltage gain to single ended output about a ground reference. The potentiometer P1 connected to the non-inverting terminal of A3 can be used to set Zero of the Pen recorder. A4 is an auxiliary amplifier while impedance matching of the multiplier to the recorder is accomplished by the operational amplifier A5. Connected as source follower.

The output of the Preamplifier is fed to a PLL which locks on to the signal frequency and is used as the reference.

A divide by two Flip – Flop SN 7473 is inserted between the phase detector and VCO. Thus the VCO frequency is twice the input frequency. The Input from the flip flop to the PSD is thus phase shifted by 90º and the PLL locks onto the carriers signal. The inputs to the Quad-2 Input exclusive OR gate SN 7486 are at the frequencies 2fc and fs. This element performs the function AB+BA and the resulting signal at the output is of the same frequency as the input signal, beating the logic output with the original signal input in the four quadrant analog multiplier 1495 followed by a low pass filter gives the required demodulated output. A buffer amplifier couples the analog multiplier to the strip chart recorder. In the detection system the

exclusive or logic and the flip-flop always gives a 90º phase shift for any frequency input. This dispenses for an extraneous tuning system.

PERFORMANCE CHARACTERISTICS

In using a PLL System for wide range of frequencies with no external tuning are has to be taken to see that it does not lock on to the harmonics of the input signal. The time constant of the low pass filter is made large enough such that the delay introduced by noise will not correlate with the noise at the signal channel.

In experimental where the depth at modulation is high there is an additional facility at waking the PLL and then allow owing the frequency to be swept while keeping the PLL disconnected from the signal channel.

The performance characteristics of the circuit are summarized in table 1. It was found that the signal to noise S/N improved by about two orders of Magnitude as compared to the signal recorded with an already existing PSD employing vacuum tubes.

Parameter	**Value**
Input Impedance	10 M Ω
Output Impedance	100 Ω
Output time constant	0.25 to 4 sec
Frequency of operation	100 KHz
DC drift (measured for 1 hour under Laboratory conditions)	0.25%
Linearity	0.1%

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